Format K1

Maharashtra State Board of Technical Education, Mumbai

TEACHING PLAN (TP)

Academic Year: **2025-26 (EVEN)**

Institute Code and Name: 0078- K. K. Wagh Polytechnic, Nashik **Semester**: Fourth
Programme and Code: Electrical Engineering (EE) **Course Index:** 404
Course and Code: Digital Electronics and Microcontroller Applications (DEM) **Course Code:** 314324
Scheme: K **Allocated Hrs.** 45 **Name of Faculty:** Ms. S.L.Sangle

CLASS: SYEE (OHM)

COURSE LEVEL LEARNING OUTCOMES (COS)

- CO1 - Apply knowledge of number system and logic circuits in working of digital system.
- CO2 - Build simple combinational and sequential circuits.
- CO3 - Access various registers in 8051 microcontrollers.
- CO4 - Develop and execute programs in assembly language for microcontroller
- CO5 - Use microcontroller in various applications.

TEACHING-LEARNING & ASSESSMENT SCHEME

Course Code	Course Title	Abbr	Course Category	Learning Scheme					Credits	Paper Duration	Assessment Scheme										Total Marks
				Actual Contact Hrs/Week			SLH	NLH			Theory				Based on LL & TSL Practical				Based on SL		
				CL	TL	LL					FA-TH	SA-TH	Total		FA-PR		SA-PR		SLA		
											Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
314324	Digital Electronics and Microcontroller Applications	DEM	SEC	3	-	4	1	8	4	3	30	70	100	40	25	10	25 @	10	25	10	175

Total IKS Hrs for Sem.: 1 Hrs

Abbreviations: CL- Classroom Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination

SUGGESTED COS - POS MATRIX FORM

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes (PSOs)		
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability and Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2	PSO-3
CO1	3	-	1	2	-	-	1	3	3	3
CO2	3	-	2	2	-	1	1	3	3	3
CO3	3	-	-	1	-	2	1	3	3	3
CO4	3	3	3	2	1	2	2	3	3	3
CO5	3	3	3	2	1	2	2	3	3	3

Legends :- High:03, Medium:02,Low:01, No Mapping: -
*PSOs are to be formulated at institute level

Maharashtra State Board of Technical Education K-1

Teaching Plan (TP)

Academic Year: 2025-26 **Institute Code:** 0078
Program: EE (OHM) **Course Code:** 314324
Course: Digital Electronics and Microcontroller Applications (DEM) **Semester:** Fourth (EE-4K)
Name of faculty: Ms.S.L.Sangle
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Chap No. (Allotted Hrs.)	CO Mention only Number	TLO Mention only Number	Unit Name and Learning Content Title/ Details	No. of Lecture	Plan (From-To)	Actual Execution (From-To)	Teaching method/ Media	Remark
1 (8)	**CO-1**	**TLO 1.1, TLO 1.2, TLO 1.3, TLO 1.4.**	**Unit - I Number System and Logic Gates** 1.1 Number System : Decimal, Binary, octal, hexadecimal, BCD. Conversion of one system into other. 1.2 Binary Arithmetic: - Addition, Subtraction (1's and 2's complement) Multiplication, Division. BCD addition. 1.3 Logic Gates: Symbol, switch circuit, logical expression, truth table of basic logic gates (AND, OR, NOT), Universal gates (NAND and NOR) and Special purpose gates (EX-OR, EX-NOR). 1.4 Arithmetic Circuits: Half and full Adder, Half and full subtractor with its truth table, boolean expression and circuits using logic gates.	**08**	**15/12/ 2025 To 01/01/ 2026**		Lecture Using Chalk-Board Presentations Video Demonstrations Flipped Classroom	
2(12)	**CO-2**	**TLO 2.1, TLO 2.2, TLO 2.3.**	**Unit - II Digital Logic Circuits** 2.1 Multiplexer and Demultiplexer: working , truth table and applications of Multiplexers and Demultiplexers. 2.2 SR Flip Flops: SR-flip flop, clocked SR flip flop with preset and clear, drawbacks of SR flip flop. JK Flip Flops: Clocked JK Flip flop with preset and clear, D and T type flip flop, Excitation table of flip flops. 2.3 Counters: Types (Asynchronous, Synchronous) and their applications.,4 bit asynchronous counter – Circuit diagram and truth table.	**12**	**05/01/ 2026 To 03/02/ 2026**		Lecture Using Chalk-Board Presentations Video Demonstrations Flipped Classroom	
3(12)	**CO-3**	**TLO 3.1, TLO 3.2, TLO 3.3, TLO 3.4.**	**Unit - III 8051 Microcontroller Architecture** 3.1 Microcomputers and microcontrollers (basic introduction and comparison). 3.2 Types of buses, address bus, data bus and control bus. Harvard and Von-Neumann architecture. 3.3 8051 Microcontroller Architecture: - Pin configuration, Register banks, bit	**12**	**04/02/ 2026 To 25/02/ 2026**		Lecture Using Chalk-Board Presentations Video Demonstrations Flipped	

			and byte addressable area, Registers: PC, DPTR, A&B, PSW and other Special function registers(SFR), I/O ports, Timers (pins and associated SFRs). 3.4 Stack and stack pointer , memory organization (RAM , ROM).				Classroom	
4(8)	**CO-4**	**TLO 4.1, TLO 4.2, TLO 4.3.**	**Unit - IV 8051 Instruction Set and Programming** 4.1 Addressing Modes: Immediate, register, direct, indirect, indexed, relative, absolute, bit inherent, bit direct. 4.2 Instruction Set (with appropriate example) : Data transfer, Logical, Arithmetic, Branching, Machine control, Stack operation, Boolean. 4.3 Assembler Directives: ORG, DB, EQU, END, CODE, DATA .	**8**	**26/02/ 2026 To 12/03/ 2026**		Lecture Using Chalk-Board Presentations Video Demonstrations Flipped Classroom	
5(5)	**CO-5**	**TLO 5.1, TLO 5.2.**	**Unit - V 8051 Interfacing and Application** 5.1 Memory interfacing - Program and Data memory 5.2 I/O Interfacing (Diagram and Flowchart) for following applications - LED, Relays, Switch, LCD, Stepper motor.	**5**	**16/03/ 2026 To 25/03/ 2026**		Lecture Using Chalk-Board Presentations Video Demonstrations Flipped Classroom	

ASSESSMENT METHODOLOGIES/TOOLS

A. Formative assessment (Assessment for Learning) (FA-TH)

- Continuous assessment based on process and product related performance indicators. Each practical will be assessed considering
  - 60% weightage is to process
  - 40% weightage to product

B. Summative Assessment (Assessment of Learning) (SA-TH)

- Continuous Assessment based on Process and Product related performance indicators. Each practical will be assessed considering
  - 60% weightage to Process
  - 40% weightage to Product

SUGGESTED LEARNING MATERIALS / BOOKS

Sr.No	Author	Title	Publisher with ISBN Number
1	R.P. Jain	Modern Digital Electronics	McGraw-Hill Publishing, New Delhi, 2009; ISBN: 9780070669116
2	V.K.Puri	Digital Electronics	McGraw Hill Education (1 July 2017); ISBN-13 : 978-0074633175
3	Salivahanan S.; Arivazhagan S.	Digital Circuits and Design	Oxford University Press India; 5th edition ; ISBN13- 978-0199488681
4	Malvino, A.P.; Leach, D.P.; Saha G.	Digital Principles and Applications	McGraw Hill Education, New Delhi, 2014, ISBN : 9789339203405

Sr.No	Author	Title	Publisher with ISBN Number
5	V. Udayashankara M. S. Mallikarjuna Swamy	8051 Microcontroller: Hardware, Software and application.	McGraw Hill Education; 1st edition; ISBN-13 : 978-0070086814
6	Kenneth Ayala	8051 Microcontroller Architecture Programming and Application	Cengage Learning India; 3rd edition ; ISBN-13 : 978-8131502006
7	Mazidi, Mohmad Ali; Mazidi, Janice Gelispe; Mckinlay Roline D.	The 8051 Microcontroller and Embedded system	Pearson Education India; 2nd edition; ISBN-13 : 978-0199681273
8	Ajay Deshmukh	Microcontroller Theory and Application	Mc Graw Hill., New Delhi,2011, ISBN-9780070585959

LEARNING WEBSITES & PORTALS

Sr.No	Link / Portal	Description
1	https://www.keil.com/download/	Simulation software
2	https://archive.nptel.ac.in/courses/108/105/108105102/	NPTEL course on-Microprocessors and Microcontrollrs
3	https://nptel.ac.in/courses/117104072	NPTEL Course-Microcontrollers and Applications, IIT Kanpur by Dr. S.P. Das
4	https://play.google.com/store/apps/details?id=com.coderbro.t	Android App for Microcontroller 8051

Note :

- Teachers are requested to check the creative common license status/financial implications of the suggested online educational resources before use by the students

Ms. S.L.Sangle
(Name & Signature of Staff)

Mr. S. B. Pawar
(Name & Signature of HOD)